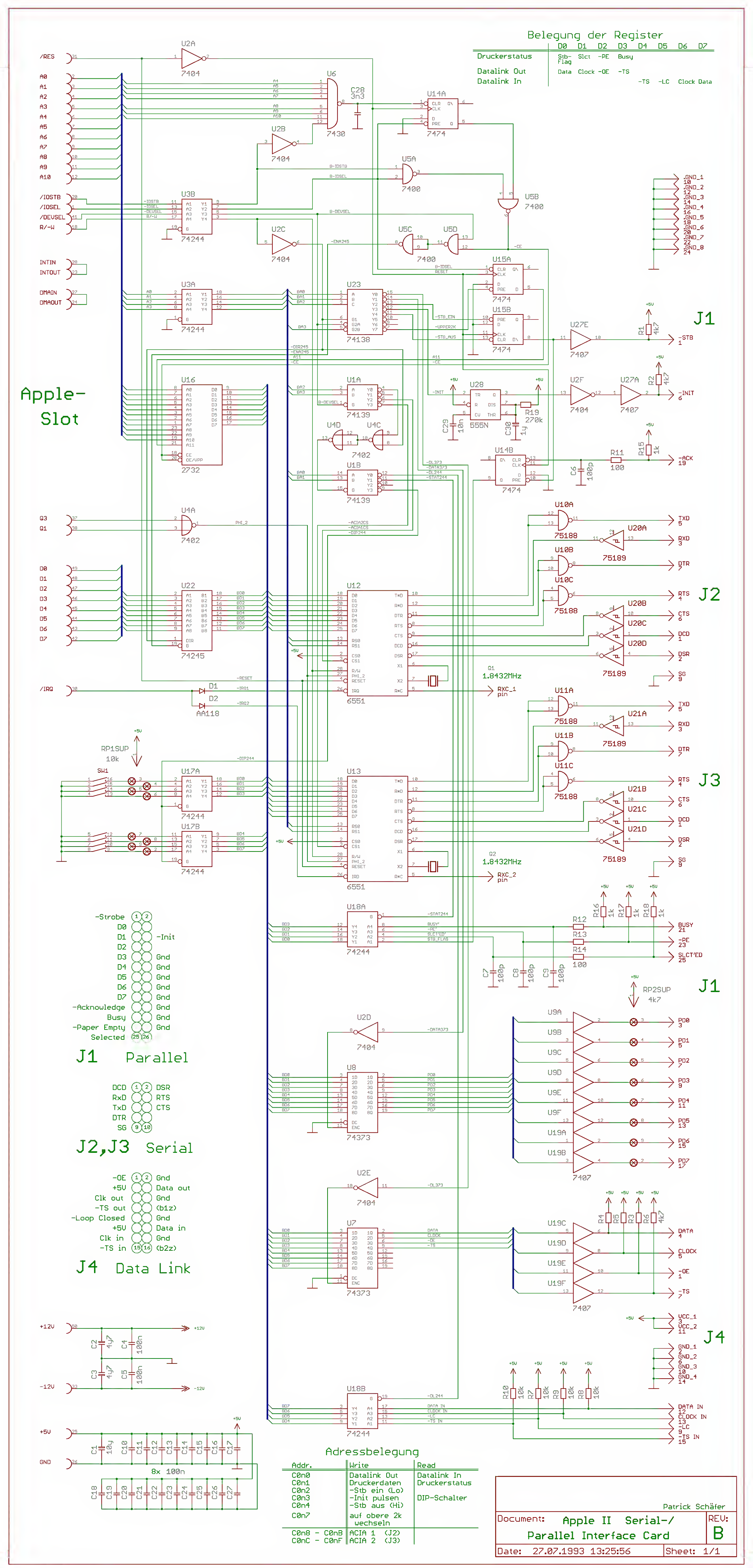
Belegung der Register
D0 D1 D2 D3 D4 D5 D6 D7
Druckerstatus Stb-Flag Slct -PE Busy
Datalink Out Data Clock -OE -TS
Datalink In -TS -LC Clock Data
Apple-Slot
J1
J2
J3
J4
Q1 1.8432MHz
Q2 1.8432MHz
-Strobe
D0
D1 -Init
D2
D3 Gnd
D4 Gnd
D5 Gnd
D6 Gnd
D7 Gnd
-Acknowledge Gnd
Busy Gnd
-Paper Empty Gnd
Selected
J1 Parallel
DCD DSR
RxD RTS
TxD CTS
DTR
SG
J2,J3 Serial
-OE Gnd
+5V Data out
Clk out Gnd
-TS out (b1z)
-Loop Closed Gnd
+5V Data in
Clk in Gnd
-TS in (b2z)
J4 Data Link
Adressbelegung
Addr. | Write | Read
C0n0 | Datalink Out | Datalink In
C0n1 | Druckerdaten | Druckerstatus
C0n2 | -Stb ein (Lo)
C0n3 | -Init pulsen | DIP-Schalter
C0n4 | -Stb aus (Hi)
C0n7 | auf obere 2k wechseln
C0n8 - C0nB | ACIA 1 (J2)
C0nC - C0nF | ACIA 2 (J3)
Patrick Schäfer
Document: Apple II Serial-/ Parallel Interface Card
REV: B
Date: 27.07.1993 13:25:56
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